Memristor emulator circuits using single CBTA

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In this paper, new analog memristor emulator circuits based on current backward transconductance amplifier (CBTA) and passive elements are proposed. They emulate both types of memristor (incremental and decremental) just by interchanging the CBTA output terminals. It uses only one CBTA, two resistors, one capacitor and one multiplier emulating grounded memristor. They consist of less CMOS transistors and have wider output ranges compared to other designed emulator circuits. The CMOS implementation of the CBTA using 0.18 μm level-7 TSMC CMOS technology parameters is also proposed. It uses 23 CMOS transistors operating with the ±0.9 V DC supply voltage. Theoretical derivations and related results are validated using SPICE simulations.

1. Introduction

Recently, the memristor, which is postulated by Chua in 1971 [1], is fabricated by using TiO2, by Hewlett-Packard (HP) laboratories [2]. There is growing interest in circuits using the memristor which have led to a great number of applications in various designs of analog electronics like chaotic oscillators, filters, sensors, cellular neural networks, and other analog circuitries.

Memristor exhibits features of both memory and neuromorphic application [3]. Since it is nonvolatile and occupies extremely small area, it is very useful for memory applications. Further, it has adjustable resistance and features of pulse-based operation for neuromorphic applications, which are suitable for adjusting the synaptic weights of neuromorphic cells. Although memristors are ideal for memory applications, their fabrication are difficult with recent technologies. Therefore, the emulators of memristor would be an alternative solution to design application circuits [see Ref. [4] and references therein].

In the literature, some of memristor SPICE macro models are proposed [5–9]. However these macromodels cannot be used in physically build real-world applications based on memristors and they are only useful for simulations. In addition, a literature survey shows that there is a large amount of research on the realization of memristors using active and passive components [3,10–14]. Such type of memristor emulators can be employed instead of memristor in many applications.

In this paper, very simple structures for emulating memristor employing only one active element namely current backward transconductance amplifier (CBTA), two resistors, one capacitor and a multiplier block are proposed. Table 1 compares the proposed memristor emulators with the previously published ones in terms of number of active and passive components, number of transistors, transistor parameter, supply voltage, and output range. It should be mentioned that the proposed circuits in Refs. [3,10,13,15,16] realize floating simulator. Mutlu and Karakulak propose grounded memristor emulator in 2010 using two opamps, a multiplier and seven passive components [11]. Because of using opamps and having higher DC power supply voltages, the simulator circuit consumes more power than the proposed one. The circuits in Refs. [13,16] employs structure similar to the proposed emulators. However the number of employed transistors in [13,16] is higher than the proposed circuits. Minaei et al. proposed memristor emulator using a non-linear resistor and 4-port adder and subtractor circuits [14]. Although the employed adder and subtractor circuits in [14] consist only 12 CMOS transistors, but the memristor emulator circuit needs a non-linear resistor and an inductor which should be realized separately. In Refs. [17,18], memristor simulator circuits are proposed which use commercially available active components such as AD844s. However, employing these components leads to high power consumption.

The rest of this paper is organized as follows. The memristor is introduced in Section 2. Section 3 presents the configurations of
The relations between four fundamental circuit elements and current (i), voltage (v), charge (q) and flux (ψ) are shown in Fig. 1 [1]. The fourth fundamental element which is called memristor (M), is based on the relationship between charge and magnetic flux.

In the memristor, the current and voltage relationship can be defined as [3]

\[ v(t) = R(t)i(t) = \frac{d\psi}{dq}(t) \]  \hspace{1cm} (1a)

where \( q(t) \) and \( \psi(t) \) denote the charge and flux, respectively, at time \( t \). Therefore resistance in time domain is defined as follows

\[ R(t) = \frac{d\psi}{dq}(s) \]  \hspace{1cm} (1b)

When the \( \psi - q \) curve is nonlinear; the resistance will vary with the operating point \( q = q_0 \) at time \( t \) on the memristor \( \psi - q \) curve. The operating point does not change without external voltage or current, hence the resistance remains constant. Thus, the signal is memorized as the resistance value of the memristor, namely, the memristance \( M \) [3].

The flux \( \psi \) is defined by \( \psi(t) = \int_{t_0}^{t} v(t)dt \). Therefore, the memristance \( M \) can be controlled by applying a voltage or current signal across the memristor, where

\[ R = M = \frac{d\psi}{dq}|_{q=q_0} \]  \hspace{1cm} (2)

3. Proposed memristor circuit and its analysis

A recent publication introduced the concept and implementation of a circuit building block termed CBTA [19]. The CBTA is proven useful in many current-mode and voltage-mode analog signal processing applications, such as voltage- and current-mode filters, oscillators, and immittance function simulators [19–27]. The circuit symbol of the proposed active element, CBTA, is shown in Fig. 2(a). Here \( p \) and \( n \) are input terminals of CBTA, \( w \) and \( z \) are output terminals of CBTA.

Fig. 2(b) shows equivalent circuit of the CBTA, which involves dependent current source at \( p, n \), and \( z \) terminals and dependent voltage source at \( w \) terminal. The terminal impedances of the ideal CBTA are infinite at \( p, n \) and \( z \) terminals and zero at \( w \) terminal. The ideal terminal voltage-current equations of the CBTA can be defined as

\[ I_z = g_{m}(V_p - V_n), V_w = V_z, I_p = I_w, I_n = -I_w. \]  \hspace{1cm} (3a)

where \( g_{m} \) is the transconductance gain of the CBTA. According to the above terminal equations, current through \( z \) terminal follows the difference of the voltages at \( p \) and \( n \) terminals multiplied by a transconductance \( g_{m} \). Hence, \( z \) terminal of the CBTA is named as non-inverting (positive) input and \( w \) terminal as inverting (negative) input, respectively. Voltage of \( w \)-terminal follows the voltage of the \( z \) terminal.

Taking the non-idealities of the CBTA into account, the above terminal equations in s-domain can be rewritten as

\[ I_z = g_{m}(s)(V_p - V_n), V_w = \mu_w(s)V_z, I_p = \zeta_p(s)I_w, I_n = -\zeta_n(s)I_w. \]  \hspace{1cm} (3b)

where \( g_{m}(s) \) is the transconductance gain of the CBTA. The parameters \( \zeta_p(s), \zeta_n(s), \mu_w(s) \) and \( g_{m}(s) \) in Eq. (3b) are the current, voltage or transconductance gains between the respective terminals. They can be expressed as:

\[ \zeta_p(s) = \omega_{m}(1 - \omega_{m})(s + \omega_{m}), \zeta_n(s) = \omega_{m}(1 - \omega_{m})(s + \omega_{m}), \mu_w(s) = \omega_{m}(1 - \omega_{m})(s + \omega_{m}), \text{ and } g_{m}(s) \]

The proposed memristor emulator circuit and their analysis. Section 4 includes the PSPICE simulation results. Conclusions are drawn in Section 5.

### Table 1
Comparison of existing circuits with the proposed circuit.

<table>
<thead>
<tr>
<th>Ref.</th>
<th># of Active Components</th>
<th># of Passive Components</th>
<th># of Transistors</th>
<th>Transistor Parameter</th>
<th>Supply Voltage</th>
<th>Output Ranges</th>
<th>Memristor</th>
</tr>
</thead>
<tbody>
<tr>
<td>[3]</td>
<td>5 OP-AMPS, 1 multiplier</td>
<td>8 R (4 Floating), 1 C</td>
<td>Too many</td>
<td>NA</td>
<td>±5</td>
<td>NA</td>
<td>Floating</td>
</tr>
<tr>
<td>[10]</td>
<td>4 AD844, 1 multiplier</td>
<td>4 R (2 Floating), 1 C</td>
<td>Too many</td>
<td>NA</td>
<td>±10</td>
<td>NA</td>
<td>Floating</td>
</tr>
<tr>
<td>[11]</td>
<td>2 OP-AMPS, 1 multiplier</td>
<td>6 R (4 Floating), 1 C</td>
<td>Too many</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
<td>Grounded</td>
</tr>
<tr>
<td>[12]</td>
<td>5 DDCC</td>
<td>4 R, 1 C</td>
<td>Too many</td>
<td>NA</td>
<td>±15 V DC Supply voltage, ( V_{p} = -0.4 ) V</td>
<td>NA</td>
<td>Floating</td>
</tr>
<tr>
<td>[13]</td>
<td>1 DDCC, 1 multiplier</td>
<td>2 R (1 Floating), 1 C</td>
<td>50 CMOS</td>
<td>NA</td>
<td>±1.25 V DC Supply voltage</td>
<td>NA</td>
<td>Grounded</td>
</tr>
<tr>
<td>[14]</td>
<td>1 Adder, 1 Subtractor, 1 Non-linear Resistor</td>
<td>1 C (1 Floating) and 1 L (1 Floating)</td>
<td>12 CMOS*</td>
<td>TSMC 0.35 μm</td>
<td>±1.25 V DC Supply voltage</td>
<td>NA</td>
<td>Grounded</td>
</tr>
<tr>
<td>[15]</td>
<td>4 CBI, 1 multiplier</td>
<td>3 R, 1 C</td>
<td>Too many</td>
<td>NA</td>
<td>±10 V DC Supply voltage, 1.6 V</td>
<td>NA</td>
<td>Floating</td>
</tr>
<tr>
<td>[16]</td>
<td>1 MO-OTA, 1 multiplier</td>
<td>1 R, 1 C</td>
<td>38 CMOS</td>
<td>TSMC 0.18 μm</td>
<td>±125 V DC Supply voltage, NA</td>
<td>Grounded</td>
<td>±10 V DC Supply voltage, NA</td>
</tr>
<tr>
<td>[17]</td>
<td>2 AD844, 1 multiplier</td>
<td>2 R, 1 C</td>
<td>Too many</td>
<td>NA</td>
<td>±10 V DC Supply voltage, 1.6 V</td>
<td>NA</td>
<td>Grounded</td>
</tr>
<tr>
<td>[18]</td>
<td>1 AD844, 1 multiplier</td>
<td>2 R, 1 C</td>
<td>Too many</td>
<td>NA</td>
<td>±10 V DC Supply voltage, 1.6 V</td>
<td>NA</td>
<td>Grounded</td>
</tr>
<tr>
<td>Prop.</td>
<td>1 CBTA, 1 multiplier</td>
<td>2 R (1 Floating), 1 C</td>
<td>23 CMOS</td>
<td>TSMC 0.18 μm</td>
<td>±10.9 V DC Supply voltage, 100 mA</td>
<td>±0.7 V</td>
<td>Grounded</td>
</tr>
</tbody>
</table>

* Only for adder and subtractor circuit.
\[ g_m \frac{O_1 + O_2}{(s + O_2)} \] where \( O_1, O_2, O_3, O_4 \) known as tracking errors are ideally equal to zero, \( g_m \) is the DC transconductance gain. In addition, \( O_2p, O_2n, O_3, O_4 \) denote corner frequencies. Note that, in the ideal case, the voltage and current gains \( (l_{w}, a_{p}, a_{n}) \) are equal to unity.

Fig. 2(c) shows the CMOS implementation of the CBTA which consists of transconductance \([28]\) and current conveyor sections \([29]\). It is obtained by connecting appropriate outputs of these sections and adjusting the dimension of CMOS transistors. The dimensions of the MOS transistors used in the CBTA implementation are given in Table 2. As seen from Fig. 2(c), the transistors \( M_{16} - M_{23} \) are used for realizing a transconductance stage, while transistors \( M_{1} - M_{15} \) form a current conveyor. In addition the current source \( I_{REF} \) and transistors \( M_{1}, M_{9} \) are employed for biasing purpose. The input voltage is defined as \( v_{in} = v_{p} - v_{n} \), and \( i_{o} \) is the output current of the transconductance stage. The output current \( i_{o} \) can be found as:

\[ i_{o} = g_m v_{in} = \left( \frac{\sqrt{2I}\rho}{K} \right) v_{in} \]

where \( K = (\mu C_{ox} W_{20,21})/(2L_{20,21}) \) is the mobility of the carrier, \( C_{ox} \) is the gate-oxide capacitance per unit area, \( W_{20,21} \) is the effective channel width, \( L_{20,21} \) is the effective channel length of the transistors \( M_{20} - M_{21} \) and \( I_{b} \) is the bias current for the transconductance stage.

The input and output terminal resistances of the CBTA can be found as follows:

\[ R_p = r_{o1}\parallel r_{o2} \]

\[ R_n = r_{o3}\parallel r_{o4} \]

\[ R_w = g_m r_{o5}\parallel r_{o6} \]

\[ R_z = r_{o7}\parallel r_{o8} \]

where \( r_{o1} \) is the output resistance of the transistors \( M_{i} \) \((i = 1, 2, \ldots, 23) \) in Fig. 2(c).

From terminal equation of the CBTA and the output of the multiplier we have

\[ v_{w} = v_{z} \text{ and } v_{w} = \eta_{z} v_{x}, v_{c} \]

where \( \eta \) is the multiplier coefficient with unity of \([V^{-1}]\). The voltages \( \eta_{z} \) and \( \eta_{c} \) are found as follows

\[ v_{x} = -I_{p} \times R = i_{in} \times R \]
\[ v_c = \frac{1}{C} \int i(t) \, dt, \text{ where } i(t) = \frac{dq_c(t)}{dt} \] (9b)

Therefore,
\[ v_c = q_c / C \] (9c)

Substituting Eqs. (8) and (9) into Eq. (7)
\[ v_{in} = i_{in} R_s + (\eta \times i_{in} R \times q_c / C) \] (10)

Therefore memristance of the proposed circuit is found as
\[ M = \frac{v_{in}}{i_{in}} = R_s + \eta \times \frac{R \times q_c}{C} = R_s \left( 1 + \eta \times \frac{R \times q_c}{R_s} \right) \] (11a)

Similar analysis can be performed for the circuit of Fig. 3(b) and the memristance value is found as
\[ M = \frac{v_{in}}{i_{in}} = R_t - \eta \times \frac{R \times q_c}{C} = R_t \left( 1 - \eta \times \frac{R \times q_c}{R_t} \right) \] (11b)

Thus the circuit of Fig. 3(b) realizes a decremental memristor. In order to avoid negative memristance value, the following condition must be satisfy
\[ R_t > \eta \times \frac{R \times q_c}{C} \] (12)

4. Non-ideal analysis

4.1. Effect of tracking errors

Taking into account the non-ideal gains of the CBTA shown in Eq. (3b), the memristance of the proposed circuit of Fig. 3(a) becomes
\[ M = \frac{v_{in}}{i_{in}} = R_s + \mu_m \times p \eta \times \frac{R \times q_c}{C} \] (13)

Normalized passive and active sensitivities of the memristance \( M \) are found as: \( S^M_p = -S^M_q = S^M_m = S^M_t = \eta = 1 \) which are no more than unity in magnitude. Thus the proposed memristor offers low passive and active sensitivities.

4.2. Effect of parasitic impedances

The basic parasitic impedance model of the CBTA is shown in Fig. 4. \( R_p, R_n, R_s \) are the input resistances and \( R_p, R_w \) are the output resistances. In addition, \( C_p, C_n \) are the input capacitances while \( C_z \) is the output capacitance.

Considering non-idealities which are shown in Fig. 4, the passive components value of Fig. 3a can be modified as follows
\[ C' = C + C_n + C_m \] (14a)

![Fig. 3. Proposed emulator circuits; (a) Incremental memristor, (b) Decremental memristor.](image)

![Fig. 4. The parasitic impedance model of the CBTA.](image)

\[ R' = R|R_p||R_m \] (14b)
\[ R_s = R_s + R_w \] (14c)

where \( R_m \) and \( C_m \) are the input resistance and capacitance of the multiplier [30].

The non-ideal memristance \( M \) including tracking errors, parasitic resistance and capacitance for the proposed simulated memristor can be refunded as
\[ M = R_s + \mu_m \times p \eta \times \frac{R \times q_c}{C} + (R_s + R_w) = (R_s + R_w) + \mu_m \times p \eta \times \frac{(R|R_p||R_m)q_c}{C + C_n + C_m} \] (15)

5. Simulation results and discussions

5.1. Non-ideal parameters of the CBTA

The characteristics of the proposed circuits have been verified using SPICE simulations. The CBTAs are simulated using the schematic implementation shown in Fig. 2c, with DC power supply voltages equal to \( V_{DD} = -V_{SS} = 0.9 \) V, bias current \( I_{BB} = 100 \mu A \) and bias current \( I_b = 100 \mu A \), which according to (4) gives \( \epsilon_m = 0.5 \) mS. The simulations are performed using 0.18 \mu m level-7 TSMC CMOS technology parameters.

The non-idealities of the CBTA are found by using the Spice simulations. The corner frequencies are found as \( \omega_{z_p} = 9610, \omega_{z_m} = 9610, \omega_{z_m} = 650 \) and \( \omega_m = 9675 \) Mrad/s and errors of these gains are \( \epsilon_{z_p} = \epsilon_{z_m} = 0.0013, \epsilon_{z_m} = -0.0013, \epsilon_{z_m} = -0.02 \) and \( \epsilon_m = -0.079 \). The maximum operating frequency of the CBTA is founded as \( f_{max} = \min(f_{z_p}, f_{z_m}, f_{z_m}, f_{z_p}) \approx 104 \) MHz.
The parasitic resistances and capacitances values of the CBTA are also founded by using the Spice simulations. They are given in Table 3.

5.2. Simulation Result of the proposed circuit

Memristor emulator circuit of Fig. 3(a) is selected for simulation test. The resistor values in the circuit are chosen as \( R_s = 10 \text{ k\ohm} \) and \( R = 100 \text{ k\ohm} \), the capacitor value and operation frequency are chosen as \((100 \text{ nF}, 100 \text{ Hz})\). AD633 from Analog Device is used as multiplier [30]. The input signal of the circuit is chosen as a sinusoidal AC source with 500 mV amplitude. Fig. 5 shows that the pinched loops of \( v-i \) relationship are obtained for the proposed memristor emulator.

To test the performance of the proposed emulator, its voltage-current characteristic is also given for \( f = 1 \text{ kHz} \) and \( f = 10 \text{ kHz} \) while \( C = 100 \text{ nF} \). The results are shown in Fig. 6(a) and (b). It can be seen that by increasing the frequency the memristor behaves like a resistor as expected.
Fig. 7. Current-voltage characteristic of the proposed memristor emulator using (a) PSPICE, (b) MATLAB, \( f = 1 \text{ Hz}, C = 10 \text{ mF} \). (c) PSPICE, (d) MATLAB, \( f = 100 \text{ kHz}, C = 100 \text{ pF} \).

Fig. 8. Offset compensated pinched hysteresis loop of proposed memristor emulator circuit.
In order to find the operating frequency of the memristor emulator circuit, the simulations are done with different capacitor and frequency values by keeping constant resistance. The results are shown in Table 4. The maximum operating frequency is founded as 460 kHz.

To compare ideal and simulation results, the mathematical calculation and the SPICE simulation are also done. Fig. 7(a) and (b) shows both the simulation and the ideal (mathematical) results for $f = 1 \text{ Hz}, C = 10 \mu\text{F}$, respectively. Fig. 7(c) and (d) shows both the simulation and the ideal (mathematical) results for $f = 100 \text{ kHz}, C = 100 \text{ pF}$, respectively.

DC offset appears in the SPICE simulation given in Figs. 5–7. The offset can be reduced using the technique given in Ref. [31]. Offset compensated pinched hysteresis loop of the proposed memristor emulator circuit is shown in Fig. 8. It is obtained by applying a DC voltage source of $-50 \text{ mV}$ amplitude to the 6th port (z-terminal) of the AD633 multiplier.

In order to demonstrate the workability of the proposed memristor emulator, it is necessary to provide the non-volatility test as well as providing the frequency-dependent pinched hysteresis loop. To demonstrate this feature, a pulse signal with a period of 1 ms, a pulse width of 0.2 ms and an amplitude of 100 $\mu\text{V}$ is applied to the proposed circuit. The time-domain simulation results for both the incremental memristor and decremental memristor circuits shown in Fig. 3 are given in Fig. 9(a) and (b), respectively.

To show transient characteristic of the proposed structure, the simulation is repeated for a sinusoidal input signal for 10 kHz sinu-
soidal input voltage with 1 V (peak to peak) amplitude. The passive components are chosen as $C = 1 \text{nF}$, $R_s = 10 \text{k}\Omega$ and $R = 100 \text{k}\Omega$. The response is shown in Fig. 10.

The voltage gain amplifiers shown in Fig. 11 are used for demonstrating the workability of the proposed circuit. The voltage gains of the circuits in Fig. 11(a) and (b) are $R / C_2 g_m$ and $M / C_2 g_m$, respectively. $R$ and $g_m$ values are chosen as 10 kΩ and 0.5 mS, respectively for Fig. 11(a). $R_s$, $R$ and $C$ values are chosen as 10 kΩ, 100 kΩ and 100 nF, respectively for Fig. 11(b). The AC and transient simulation results are given in Figs. 12 and 13, respectively, which confirm the performance of the proposed emulator circuit.

Further, the step response of the proposed memristor emulator circuit is also investigated. The unit step waveform is applied to a resistor–capacitor (RC) circuit which component values are 10 kΩ and 100 nF as shown in Fig. 14(a) [32]. The resistor in Fig. 14(a) is replaced with a memristor as shown in Fig. 14(b) and the same input is applied. The simulation results of RC and memristor–capacitor (MC) circuits are shown in Fig. 15.
6. Conclusions

In this paper, memristor emulator circuits are proposed using only one CBTA as active element. They also consist of one multiplier, one grounded capacitor and two resistors. The proposed circuits offer the following advantageous features: (i) Use of single active component which means less power consumption. Since power consumptions are important for the circuit designers, they...
look for simple structures employing no more than a single active element; (ii) use of grounded capacitor; (iii) Low active and passive sensitivities.

In addition, the CMOS implementation of the CBTA consists of only 23 CMOS transistors operating with the ±0.9 V DC supply voltage. The proposed circuits use less CMOS transistors and have wider output ranges compared to other designed emulator circuits. The simulations are performed using SPICE based on 0.18 μm level-7 TSMC CMOS technology parameters. It is observed that the theoretical and simulation results are in good agreement.

References