Unity/Variable-gain Voltage-mode/Current-mode First-order All-pass Filters Using Single Dual-X Second-generation Current Conveyor

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ABSTRACT

In this paper, two new general topologies for realizing voltage-mode (VM)/current-mode (CM) first-order all-pass filter transfer functions (TFs) are presented. The proposed topologies use single dual-X second-generation current conveyor (DXCCII) and three impedances $Z_1$, $Z_2$, and $Z_3$. Based on the selection of $Z_1$, $Z_2$, and $Z_3$, new VM and CM all-pass filters with unity or variable gains are obtained. The proposed VM/CM filters have high-input/high-output impedances which provide easy cascading at their input/output terminals, respectively. Non-ideal gain and parasitic impedance effects, associated with actual DXCCII implementation, on the performance of the developed topologies are also included. Finally, simulation program with integrated circuit emphasis (SPICE) simulation results based on level 49, 0.25 µm TSMC complementary metal-oxide-semiconductor (CMOS) technology parameters are given to confirm the theory.

Keywords: All-pass filter, CMOS, Current-mode, Dual-X second-generation current conveyor, Variable gain, Voltage-mode.

1. INTRODUCTION

The dual-X second-generation current conveyor (DXCCII) is a versatile active element which can be used for implementing either voltage-mode (VM) or current-mode (CM) functions [1,2]. Some applications of the DXCCII, such as VM and CM second-order multifunction filters, oscillator and gyrator, have been reported in [1-4]. However, to the best knowledge of the authors no DXCCII-based realization of the first-order all-pass filter has been proposed so far.

All-pass filters find wide applications in analog signal processing to shift phase of the signal while keeping its amplitude constant over the frequency range. In addition, they can be used to equalize the undesired phase change as a result of processing the signal. It is well known that a topology consisting of only grounded passive elements is advantageous from integrated circuit (IC) realization point of view [5-7].

Although operational amplifiers (op-amps) and passive elements can be used to construct all-pass filters [8,9], they suffer from the limited gain-bandwidth product of the op-amp. Fortunately, realization of the first-order all-pass filters using current conveyors (CCs) has received considerable attention in the technical literature [10-33]. The advantages and drawbacks of these first-order all-pass filters can be summarized as follows.

The proposed VM circuits in [10] use single, positive-type, second-generation current conveyor (CCII+) and three to five passive elements but they do not guarantee high input impedance. Higashimur and Fukui proposed VM and CM all-pass filters, respectively, in [11] and [12], employing single, negative-type, second-generation current conveyor (CCII−). Although the proposed filters in [11] and [12] offer high input and high output impedances, respectively, they suffer from employing floating capacitors as well as resistor matching requirement and unity gain. In [13] new CM/VM all-pass filters using single CCII+/CCII−, four resistors and single grounded capacitor were proposed. These filters have high input/high output impedances in VM/CM operations, but they suffer from a constant gain of 0.5. The CC-based VM filters proposed in [14-17] use a floating capacitor and have frequency-dependent input impedances. The first-order all-pass filter given in [18] which employs a third-generation current conveyor (CCIII) operates in transadmittance mode (TAM) (i.e. input as voltage and output as current) and does not offer high input impedance. Also, very simple VM first-order all-pass filters using one differential difference current conveyor (DDCC), one grounded capacitor and one floating resistor were presented in [19] and [20], but their input impedances depend on the values of the employed passive elements. Similarly, a single DDCC-based all-pass filter with a floating capacitor and grounded resistor was presented in [21]. However, the input impedance of this circuit is also frequency-dependent. Recently, two
new VM all-pass filter using single dual-output current conveyors (DO-CCIIs) and single modified negative type current conveyor (MCCII) were reported in [22] and [23], respectively. These circuits provide high input impedance and employ one grounded capacitor but two floating resistors.

The CM and VM all-pass filters in [24] and [25] employ two CCIIs and four grounded passive elements. The VM filters in [26-28] use only grounded passive elements but require two differential voltage current conveyors (DVCC), and the CM circuit in [29] requires two CCIIs and employs a floating capacitor. The CM all-pass filters in [30] employ single DVCC together with three passive elements but they do not provide gain and employ at least one floating passive element. The CM all-pass circuit with high output impedance reported in [31,32] employs single active element but requires two identical input currents. Thus, an additional active element should be used to provide these identical input currents. Another CM all-pass filter reported in [33] employs only grounded passive elements but requires two differential voltage current conveyors (DVCC), and the CM circuit in [29] requires two CCIIs but require two differential voltage current conveyors (DVCC), and the CM circuit in [29] requires two CCIIs and employs a floating capacitor. The CM all-pass filter based on an active element, namely, Z-copy current inverter transconductance amplifier (ZC-CITA), and only one grounded capacitor was reported in [34]. The ZC-CITA is composed of a dual-output operational transconductance amplifier (OTA), a current mirror and a current inverter circuit.

In this paper, novel VM and CM first-order all-pass filters using a single DXCCII and four passive components, (grounded capacitor(s) and grounded or floating resistors), are proposed. The proposed all-pass filters possess attractive features such as using single active component, low sensitivities, variable gain (some of them), use of only grounded capacitor(s) and high input impedance (high output impedance) for VM (CM) realizations. Non-ideal gain and parasitic impedance effects of the DXCCII on the transfer functions (TFs) of the proposed filters are investigated.

2. DXCCII AND PROPOSED CIRCUITS

The DXCCII, whose symbol is shown in Figure 1, is an active element ideally defined with following voltage-current terminal relationships:

\[ I_y = 0, I_{zp} = I_{xp}, I_z = I_{xn}, V_{zp} = V_{xp}, V_{zn} = -V_{yn} \]  

(1)

However, including its non-ideal voltage and current gains as well as parasitic impedance effects, the DXCCII can be characterized by the following matrix equation:

\[
\begin{bmatrix}
I_y \\
I_{zp} \\
I_x \\
V_{zp} \\
V_{xn}
\end{bmatrix} =
\begin{bmatrix}
0 & 0 & sC + \frac{1}{R_y} & 0 & 0 \\
0 & 0 & 0 & sC + \frac{1}{R_p} & 0 \\
0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 \\
0 & Z_{zn}(s) & -\beta(s) & 0 & 0
\end{bmatrix}
\begin{bmatrix}
I_y \\
I_{zp} \\
I_x \\
V_{zp} \\
V_{xn}
\end{bmatrix} +
\begin{bmatrix}
I_{xp} \\
V_{yn}
\end{bmatrix}
\]  

(2)

Here, \( \alpha(s) = \alpha(1 + s/\omega_{in}) \) and \( \beta(s) = \beta(1 + s/\omega_{in}) \) \((i = 1, 2) \) are the frequency-dependent non-ideal current gains and voltage gains, respectively. The DC non-ideal gains, \( \alpha_0 \) and \( \beta_0 \), are ideally equal to unity and their bandwidths, \( \omega_{in} \) and \( \omega_{in} \), are ideally equal to infinity. It is obvious that the Z- and Y-terminal parasitic resistors (\( R_z \), \( R_y \)) and capacitors (\( C_z \), \( C_y \)) are ideally equal to infinity and zero, respectively. The X-terminal parasitic impedance \( Z_x(s) = R_x + sL_x \) is ideally equal to zero where \( R_x \) and \( L_x \) are called the X-terminal parasitic resistor and inductor, respectively.

The proposed configurations for realizing VM and CM all-pass filters are shown in Figures 2 and 3, respectively. Assuming ideal DXCCII, routine analysis of the circuits in Figures 2 and 3 gives the following TF:

\[ \frac{V_{out}}{V_{in}} = \frac{I_{out}}{I_{in}} = \frac{Z_3}{Z_3 - Z_1} \]  

(3)

2.1 VM First-order All-pass Filters

Selecting different impedances for \( Z_1 \), \( Z_2 \), and \( Z_3 \) in Figure 2, one can obtain two VM all-pass filters as follows.

a) VM circuit 1: If \( Z_1 = R, Z_2 = 1/(sC) \) and \( Z_3 = (R) \| (1/(sC)) \) are chosen, a unity-gain, non-inverting, all-pass with following TF is obtained.

\[ \frac{V_{out}}{V_{in}} = \frac{1 - sCR}{1 + sCR} \]  

(4)

The filter in frequency domain has the following phase response in ideal case:

\[ \phi(\omega) = -2 \tan^{-1}(\omega CR) \]  

(5)

Figure 1: Symbolic representation of the DXCCII.
Note that by interchanging the resistor and capacitor at terminals \( X_p \) and \( X_n \), a unity-gain inverting all-pass filter can be obtained as

\[
\frac{V_{out}}{V_{in}} = -\frac{1 - sCR}{1 + sCR}
\]

which has a phase response in frequency domain as

\[
\phi(\omega) = 180^\circ - 2 \tan^{-1}(\omega CR)
\]

The proposed VM circuits have the advantage of using only grounded passive elements, which is a desired feature in integrated circuit (IC) implementation.

b) VM circuit 2: If \( Z_1 = R_1, Z_2 = R_2 + 1/(sC) \) and \( Z_3 = R_3 \) are chosen, the TF in Equation (3) becomes

\[
\frac{V_{out}}{V_{in}} = \frac{R_3}{R_1} \frac{1 - sC(R_1 - R_2)}{1 + sCR_2}
\]

Selecting \( R_1 = 2R_2 \) results in a gain-variable non-inverting first-order all-pass filter as:

\[
\frac{V_{out}}{V_{in}} = \frac{R_3}{R_1} \frac{1 - sCR_2}{1 + sCR_2}
\]

Therefore the phase response of the filter in frequency domain can be given by

\[
\phi(\omega) = -2 \tan^{-1}(\omega CR_2)
\]

Note that by selecting \( Z_1 = R_1 + 1/(sC), Z_2 = R_2 \) and \( Z_3 = R_3 \) with \( R_2 = 2R_1 \), a gain-variable inverting all-pass filter with following TF and phase response in frequency domain can be obtained:

\[
\frac{V_{out}}{V_{in}} = -\frac{R_3}{R_2} \frac{1 - sCR_1}{1 + sCR_1}
\]

It should be mentioned that the gain of the filters with TFs in Equations (9) and (11) can be controlled by changing \( R_3 \) without disturbing their phase responses.

### 2.2 CM First-order All-pass Filters

Similar to the VM filters discussed in Section 2.1, selecting different impedances for \( Z_1, Z_2 \) and \( Z_3 \) in the circuit of Figure 3 results in CM all-pass filters as follows.

a) CM circuit 1: If \( Z_1 = R, Z_2 = 1/(sC) \) and \( Z_3 = R || 1/(sC) \) are chosen, the following CM TF is found.

\[
\frac{I_{out}}{I_{in}} = \frac{1 - sCR}{1 + sCR}
\]

Therefore, a unity-gain non-inverting all-pass filter is obtained. Note that by interchanging the resistor and capacitor at terminals \( X_p \) and \( X_n \), an inverting all-pass filter with unity gain is obtained as

\[
\frac{I_{out}}{I_{in}} = -\frac{1 - sCR}{1 + sCR}
\]

The phase responses of the TFs in Equations (13) and (14) are same as given in Equations (5) and (7), respectively. As mentioned for the VM circuit 1, the proposed CM filter uses only grounded passive elements, thus making it attractive from IC implementation point of view.

b) CM circuit 2: If \( Z_1 = R, Z_2 = R + 1/(sC) \), and \( Z_3 = R \) are chosen, a non-inverting, gain-variable filter with the following CM TF is obtained:

\[
\frac{I_{out}}{I_{in}} = \frac{R_3}{R_1} \frac{1 - sC(R_1 - R_2)}{1 + sCR_2}
\]

Selecting \( R_1 = 2R_2 \) results in a first-order CM all-pass filter TF as:
\[
\frac{I_{out}}{I_{in}} = \frac{R_3}{R_1} \frac{1 - sCR_2}{1 + sCR_2}
\]

(16)

Note that by selecting \(Z_3 = R_3 + 1/(sC)\), \(Z_2 = R_2\), and \(Z_1 = R_1\) with \(R_3 = 2R_2\), an inverting, gain-variable, all-pass filter is obtained as

\[
\frac{I_{out}}{I_{in}} = \frac{R_3}{R_2} \frac{1 - sCR_1}{1 + sCR_1}
\]

(17)

The phase responses of the TFs in Equations (16) and (17) are the same as given in Equations (10) and (12), respectively. Hence, the gain of these CM filters can be controlled by changing \(R_3\) without disturbing their relevant phase responses. Finally, it should be mentioned that the grounded and floating resistors of the proposed circuits can be realized using electronically controllable CMOS-based grounded and floating resistors reported in [35] and [36], respectively.

3. NON-IDEALITY AND MISMATCHING EFFECTS

In this section, non-ideality effects of the DXCCII (non-ideal gain and parasitic effects) and mismatching effects of the passive elements on the TF of the proposed all-pass filters are investigated. If non-ideal gains of the DXCCII in the all-pass filters in Figures 2 and 3 are taken into account (i.e. matrix Equation (1) with only non-ideal gains), the TF in Equation (3) becomes

\[
\frac{V_{out}}{V_{in}} = \frac{I_{out}}{I_{in}} = Z_3\alpha_1(s)\beta_1(s) - Z_2\alpha_1(s)\beta_2(s)
\]

(18)

As an example, if \(Z_1 = R_1\), \(Z_2 = 1/(sC)\) and \(Z_3 = R_2 \parallel 1/(sC)\) are chosen for the TF in Equation (18), the following TF is realized:

\[
\frac{V_{out}}{V_{in}} = \frac{I_{out}}{I_{in}} = \frac{\alpha_1(s)\beta_1(s) - sCR\alpha_2(s)\beta_2(s)}{1 + sCR}
\]

(19)

It is observed from Equations (20) and (21) that only if \(Z_3 = R_3\), \(Z_2 = 1/(sC)\) and \(Z_1 = R_1 \parallel 1/(sC)\) are chosen for the circuits in Figures 2 and 3, the X-terminal parasitic resistor \(R_2\) along with the capacitor \(C\) brings extra poles/zeros to the TFs which can restrict the high frequency operation of the circuit [39]. In fact, the proposed VM and CM circuits of type 2 suffer less from parasitic resistance at X-terminals than the proposed circuits of type 1 because in type 2 circuits, \(R + 1/sC\) impedances are connected at X-terminal and hence the resistor can be floating followed by a grounded capacitor and in this case, the parasitic resistance at X-terminal can be easily absorbed by added physical resistor and by making good characterization for the designed DXCCII. The low frequency performances of the proposed circuits are not affected from the parasitic impedances, since there is no single grounded capacitor connected to the \(Z\) terminals in the proposed VM or CM filters [7]. Finally, if unmatched capacitors and resistors are selected in Equation (18) as \(Z_1 = R_1\), \(Z_2 = 1/(sC)\) and \(Z_3 = R_2 \parallel 1/(sC)\), the following TF is obtained:

\[
\frac{V_{out}}{V_{in}} = \frac{I_{out}}{I_{in}} = \frac{R_2\alpha_1(s)\beta_1(s)}{R_1} \frac{1 - sCR_2\alpha_2(s)\beta_2(s)}{1 + sCR_2}
\]

(22)

It is observed from Equation (22) that for realizing a unity-gain, all-pass filter with a pole frequency of \(f_p = 1/(2\pi R_2\omega_0)\), one should select \(C_2 = C\alpha_2(s)\beta_2(s)\) and \(R_2 = \frac{1}{\alpha_2(s)\beta_2(s)}\), where operating frequency of the proposed all-pass filter is assumed to be much smaller than pole frequencies of non-ideal gains of the DXCCII.

4. SIMULATION RESULTS AND DISCUSSION

Simulation program with integrated circuit emphasis (SPICE) simulation program is used to test the performance of the proposed circuits. The complementary metal-oxide-semiconductor (CMOS) internal structure of the DXCCII used in the simulations is shown in Figure 4 [40] with transistor dimensions given in Table 1. Simulations are based on level 49, 0.25 μm TSMC CMOS technology parameters [41]. The supply voltages and
Figure 4: CMOS structure of the DXCCII [40].

Figure 5: Magnitude and phase responses of the first and second VM all-pass filters.

Figure 6: Time-domain responses of the proposed VM all-pass filters.
compensation capacitors are selected as $V_{DD} = V_{SS} = 1.25$ V, $V_p = -0.3$ V, and $C_{C1} = C_{C2} = 0.6$ pF. The VM all-pass filters with a pole frequency of $f_o = 1.59$ MHz and unity gain are obtained by selecting $R = 1$ kΩ and $C = 0.1$ nF for the first circuit as well as $R_1 = R_3 = 2$ kΩ, $R_2 = 1$ kΩ and $C = 0.1$ nF for the second one.

Both the ideal and simulated phase and magnitude responses of the proposed VM all-pass filters are shown in Figure 5. The output noise and equivalent input noise of the first VM circuit are found to be $2.473 \times 10^{-8}$ V/√Hz and $2.91 \times 10^{-8}$ V/√Hz, respectively, at frequency of 1.59

<table>
<thead>
<tr>
<th>MOS transistors</th>
<th>$W$ (µm)/$L$ (µm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>$M_1, M_2, M_3, M_4$</td>
<td>2/0.25</td>
</tr>
<tr>
<td>$M_{15}, M_{16}, M_{17}, M_{18}, M_{19}, M_{20}$</td>
<td>2/0.25</td>
</tr>
<tr>
<td>$M_5, M_6, M_7, M_8, M_9, M_{10}$</td>
<td>4/0.25</td>
</tr>
<tr>
<td>$M_{11}, M_{12}, M_{13}, M_{14}$</td>
<td>16/0.25</td>
</tr>
</tbody>
</table>

Figure 7: THD variation of the proposed VM all-pass filters against input voltage (peak).

Figure 8: Magnitude and phase responses of the first and second CM all-pass filters.

Figure 9: Time-domain responses of the proposed CM all-pass filters.
MHz. The output and equivalent input noise values for the second VM filter are evaluated as 3.824 × 10⁻⁸ V/√Hz and 5.246 × 10⁻⁸ V/√Hz, respectively. The time-domain responses of the proposed VM filters at 1.59 MHz are shown in Figure 6. The discrepancy between ideal and simulated results can be attributed to the non-ideal gain and parasitic impedance effects of the DXCCII. The variation of the total harmonic distortion (THD) versus applied sinusoidal input voltage for both of the proposed CM all-pass filters are calculated as 3.29 and 4.127 × 10⁻⁸ V/√Hz, respectively, at frequencies of 1.59 MHz and unity gain by selecting R = 1 kΩ and C = 0.1 nF for the first circuit as well as R = 1 kΩ and C = 0.1 nF for the second one. Both the ideal and simulated phase and magnitude responses of the proposed CM filters are depicted in Figure 8. Comparing Figures 5 and 8 demonstrates that the second VM filter has better THD performance than the first one.

Similarly, CM all-pass filters are simulated for a pole frequency of f = 1.59 MHz and unity gain by selecting R = 1 kΩ and C = 0.1 nF for the first CM filter with a 1 kΩ resistive load are calculated as 3.29 × 10⁻³ V/√Hz and 4.127 × 10⁻¹1 A/√Hz, respectively, at frequency of 1.59 MHz. For the same conditions, the second CM filter exhibits output and equivalent input noises of 2.037 × 10⁻⁸ V/√Hz and 2.661 × 10⁻¹¹ A/√Hz, respectively. The time-domain responses of the proposed CM filters at 1.59 MHz are shown in Figure 9. The variations of the THD against applied sinusoidal input current for both of the proposed CM all-pass filters at f = 1.59 MHz are given in Figure 10, where the biasing currents of the DXCCII are the same as given for the VM filters. It can be seen that the first CM filter exhibits better THD performance than the second one. Moreover, the total power dissipation of the proposed VM and CM circuits are found to be approximately 2.1 mW.

5. CONCLUSION
In this study, novel VM and CM first-order all-pass filters with unity/variable gains employing a single DXCCII are proposed. The developed VM and CM filters have high input impedances and high output impedances, respectively, and use grounded capacitor(s); thus, they are suitable for IC implementation. The non-ideality analyses of the introduced filters are given. The simulation results are in close proximity with the theoretical ones, whereas the discrepancy between them arises from the effects of non-ideal gains and parasitic impedances of the DXCCII.

REFERENCES

AUTHORS

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